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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:

Russell E. Henning

Serial No.: 09/751,129

Filed: December 29, 2000

For: Providing Error Resilience and
Concealment for Video Data

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Art Unit: 2613

Examiner: Anand S. Rao

Atty Docket: ITL.0501US
P10387

Assignee: Intel Corporation

8/1/05
NOTED
AR

Mail Stop **Appeal Brief-Patents**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY BRIEF

This responds to the new points raised by the Examiner in the Examiner's Answer.

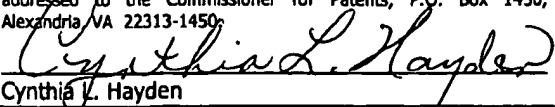
Claim 1

Claim 1 *inter alia* calls for using different error resilience techniques with different frames. Specifically, the second error resilience technique "to replace the bit pattern for the second type of frame with a shorter bit pattern."

In the illustrated embodiment of the present specification, it is the variable length coder (VLC) block 255 that provides the shortened bit pattern. It replaces frequently occurring bit patterns with codes of shorter length, thereby reducing the total number of bits to be transmitted. See page 11, lines 13-16.

Date of Deposit: May 17, 2005

I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.


Cynthia L. Hayden